What is claimed is:

1. A method of manufacturing built-in capacitors in the multi-layer substrate, said method comprising:

forming a plurality of via holes in said multi-layered substrate, said multi-layered substrate comprising a first dielectric layer, a second dielectric layer, and a third dielectric layer, said second dielectric layer having two second conductive layers being respectively mounted on a top and a bottom surface to pattern as power plane and ground plane, said first dielectric layer, and said third dielectric layer having respective a first conductive layer and a third conductive layer ;

filling a capacitor dielectric material into a portion of said via holes, which are predetermined design as capacitors, said capacitor dielectric material having a dielectric constant substantially higher than said second dielectric layer;

curing said capacitor dielectric material;

masking a dry film on areas of said second conductive layers where those are desired regions to form a copper layer thereon;

etching away exposed regions of said second conductive layers so as to form ground plane and power plane;

removing said dry film;

electroplating two copper layers respectively on said ground plane and power plane to seal said copper dielectric material to form built-in capacitors;

assembling and sintering said first conductive layer/ said first

dielectric layer/ said ground plane/said second dielectric layer/said power plane/said third dielectric layer/ said third conductive layer together;

patterning said first conductive layer and said third conductive layer to form connective trace layers; and

performing a plating through hole process to connect said via holes to said connective trace layers and said power plane and ground plane.

2. The method of claim 1, further comprising at least one power ring and one ground ring on one of said connective trace layers, said at least one power ring and one ground ring respectively connecting to said power plane and ground plane.

3. The method of claim 1, further comprising filling another capacitor dielectric material into said via holes to form capacitors with different capacitance.

4. A multi-layered substrate structure, comprising:

a assembled board with a top conductive trace layer/ a first dielectric layer/ a ground plane/ a second dielectric layer/ a power plane/ a third dielectric layer/ a bottom conductive trace layer stack, said assembled board having a plurality of plated through holes therein; and

said ground plane/ said second dielectric layer/ said power plane containing at least one built-in capacitor, said built-in capacitor being formed of a capacitor dielectric material in said plated through holes of said second dielectric layer and having copper layers as capacitor plates,

said capacitor dielectric material having a dielectric constant substantially higher than that of said second dielectric layer, still said top conductive trace layer comprising a power ring and ground ring, respectively, connecting said power plane and said ground plane.

5. The multi-layered substrate according to claim 4, further comprising another capacitor dielectric material in said plated through holes of said second dielectric layer to form capacitors with different capacitance.

6. The multi-layered substrate according to claim 4, wherein in said multi-layered substrate is for PCB, BGA supporting, or flip-chip build-up substrate use.